CONTROL DATA® 6400/6500/6600 EXTENDED CORE STORAGE SYSTEMS

Reference Manual

RECORD of REVISIONS

REVISION	NOTES
A	Manual released.
(2-16-68)	

FORM CA230 REV. 1-67
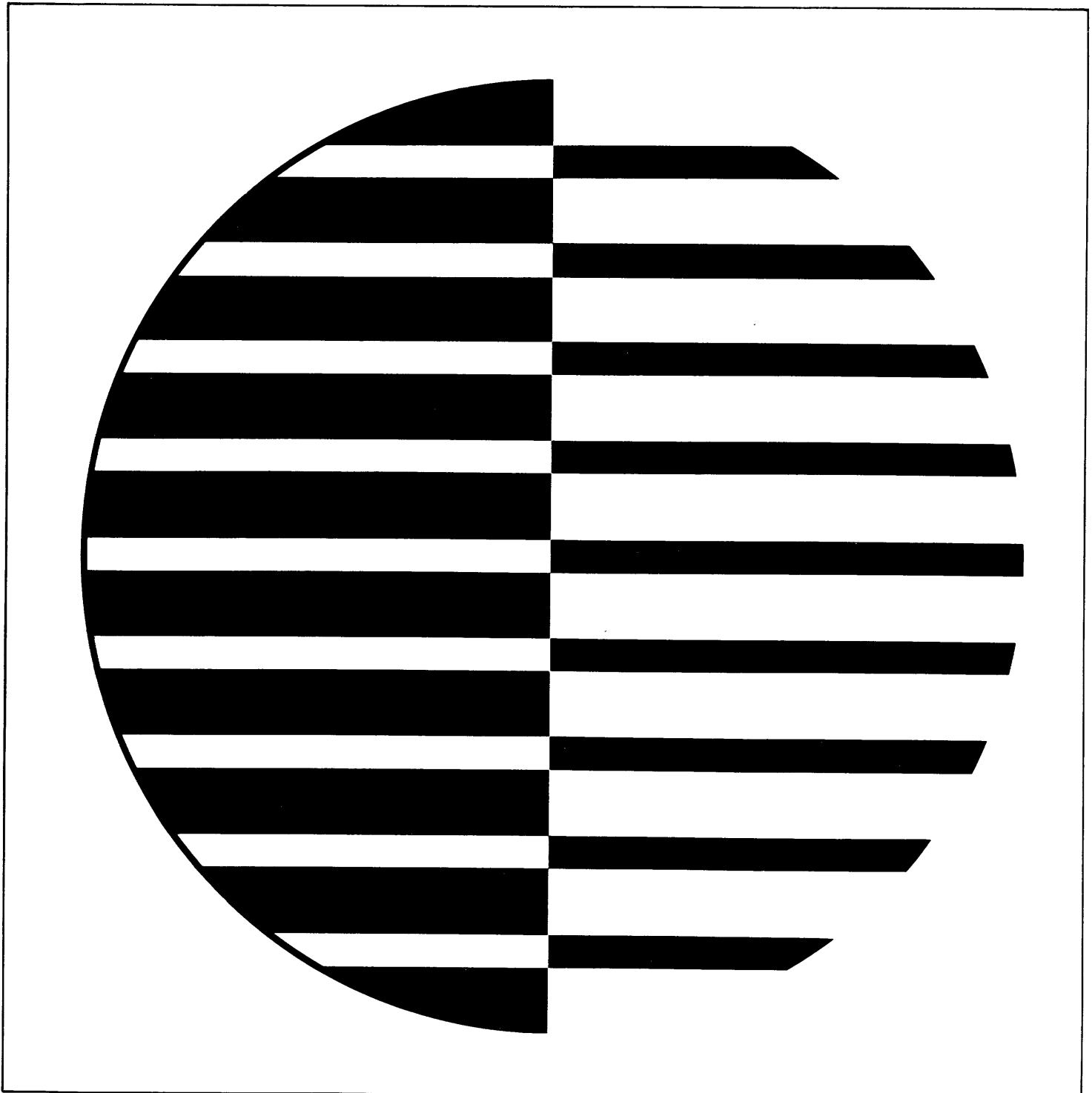
FOREWORD

This manual assumes familiarity with the CONTROL DATA® 6400/6500/6600 Computer Systems Reference Manual, Pub. No. 60100000.
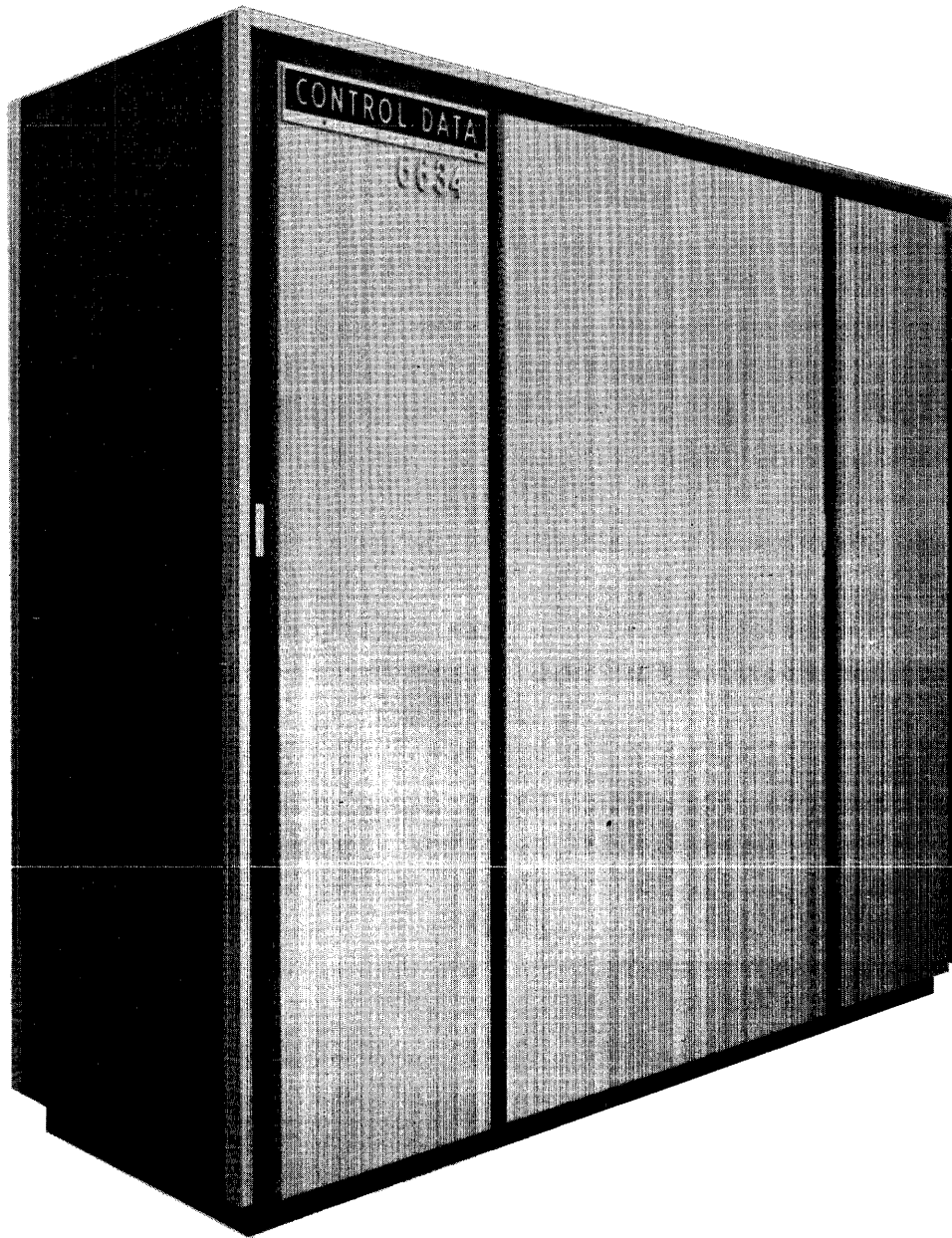
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TYPICAL EXTENDED CORE STORAGE SYSTEM

The CONTROL DATA® 6633 Extended Core Storage (1 bank), 6634 Extended Core
Storage (2 bank), and 6635 Extended Core Storage (4 bank) configurations all
occupy the same cabinet which is shown above. The CONTROL DATA® 6636
Extended Core Storage (8 bank) requires two such cabinets.

1. EXTENDED CORE STORAGE ASSEMBLY

Extended Core Storage (ECS) is a random-access word-organized memory of up to two million 60-bit words. The system can be accessed by up to four CONTROL DATA® 6000 Series computers. A maximum transfer rate of one 60-bit word every 100 nsec (10 MHz) is possible.

SUMMARY OF CHARACTERISTICS

The following summary lists characteristics of an Extended Core Storage configuration.

- Bounds protection and relocation capabilities for ECS

- 125,952 60-bit words per bank (minimum available size)

- Available in 1-, 2-, 4-, 8-, or 16-bank configurations (maximum size is 2,015,232 60-bit words)

- Memory organized in logically independent banks of 488-bit words (eight 60-bit words plus parity bit for each) with corresponding multiphasing of banks

- Reserve memory to minimize down-time

- A cycle time of 3.2 μsec per bank (read/write time for 488-bit word)

- Four access channels for communication with up to four, and any combination of CDC® 6400, 6500, 6600, or 6416 systems

- Scanning mechanism services all channels equally and sequentially. Scanning occurs after each record of eight 60-bit words

- Assembly/disassembly (60-bit words into 480-bit word plus 8-bit parity and vice versa)

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- Parity bit generated for each 60-bit word; parity check on Read operations

- Computer to computer communication without memory references

- Hardware degradation that allows the customer to retain half of his system in case of an ECS failure*

- Self contained refrigeration system

GENERAL CONFIGURATION

An Extended Core Storage configuration for a 6400, 6500, 6600, or 6416 involves three logical elements: Extended Core Storage, Extended Core Storage Controller, and Extended Core Storage Coupler. The logical elements are shown in Figure 1-1.
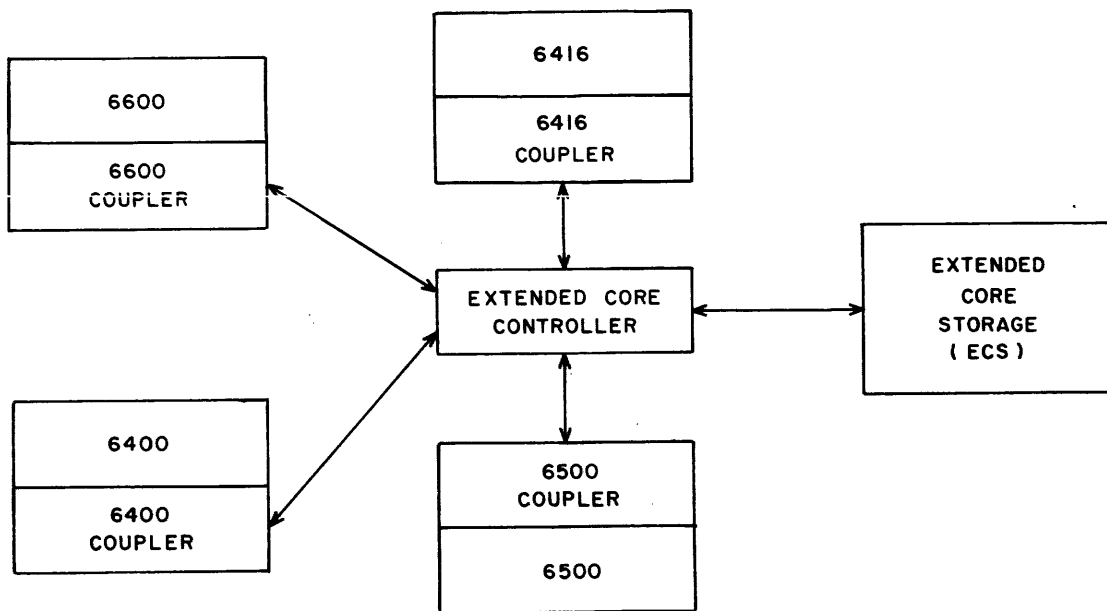
Figure 1-1. Typical Extended Core Storage Configuration

*For ECS systems with 250K words or more.

Extended Core Storage

The ECS unit provides up to two million directly addressable 60-bit words. Eight 60-bit words are organized into a 488-bit data word in ECS (Figure 1-2). A parity bit is attached to each 60-bit word in the controller on a Write ECS.
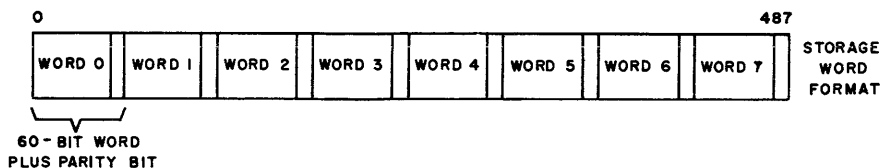
Figure 1-2. ECS Word Format

Although all transfers are basically for eight 60-bit words, any number of words may be transferred. ECS is organized into banks of 125,952 60-bit words per bank. The minimum available ECS is a bank of 125,952 60-bit words. Expanding ECS to four banks provides a bay containing 503,808 60-bit words. Four bays provide the maximum available ECS capability of 2,015,232 60-bit words. Within this range of minimum to maximum (125K to 2000K), ECS is available in 1-, 2-, 4-, 8-, or 16-bank configurations.

ECS is contained in a cabinet similar to the 6000 Series computers. Each cabinet contains a refrigeration system similar to the 6000 Series computers. One bay (four banks) fills one cabinet. A four-bay (16 bank) system takes four cabinets. The cabinet for each bay is completely self-contained. The one and two bank sizes are housed in the same cabinet as a full bay.

A maximum transfer rate of one 60-bit word every 100 nsec can be attained if at least four banks (500K) of ECS and 65K of Central Memory are available in the system. If Central Memory has less than 65K then the coupler will wait between eight-word records.

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If less than 500K of ECS is available, the controller (and therefore the coupler) will wait between the records.

An assembly/disassembly network in ECS assembles eight 60-bit words (plus eight parity bits) into a 488-bit word for Write operations. On Read operations, this network dissassembles eight 60-bit words and their associated parity bits from the 488-bit word read from ECS. Each bank has an assembly/disassembly network.

Each bank has a read/write cycle time of 3.2 μsec per 488-bit word selected. This storage cycle time is diagrammed in Figure 1-3.
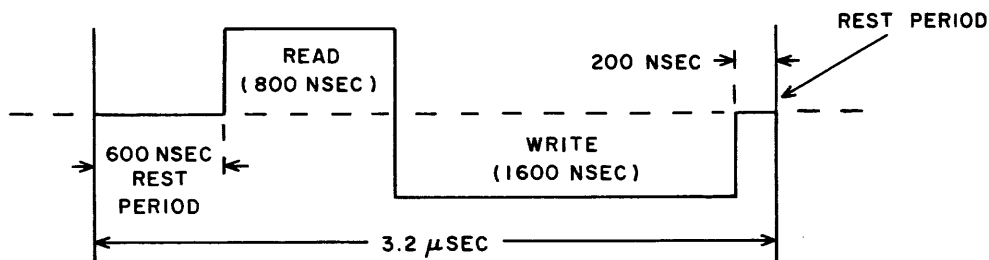
Figure 1-3. ECS Read/Write Cycle

Each ECS bank has 5K of reserve memory locations to minimize down-time. This ensures the customer a full, contiguously addressable 125K of memory even though a bank may develop some bad locations. The 5K of reserve memory is usable in 1K increments. To exchange one reserve increment with 1K of memory requires the interchanging of two wires.

ECS has maintenance hardware that enables it to run independently of the controller. It is also possible, in configurations of 250K or more, to release half of the ECS system for maintenance and to retain the other half for the system. In the 2-, 8-, and 16-bank systems, the released half of ECS can be run in Maintenance mode.

Extended Core Storage Controller

The ECS Controller provides four bi-directional access channels to read or write 60-bit data words, a scanning mechanism to service the requests of these channels, a parity generator and checker, and the associated control necessary to time these operations. The controller also contains an 18-bit Flag register that may typically be used for communication by the attached computers.

Scanner and Access Channels

Bi-directional access channels on the controller provide the paths for data and control signals between ECS and the coupler. To permit access to ECS by other systems, a total of four access channels are provided. Data trunks in the access channels are 60 bits wide.

Data transfer (for block transfers) is accomplished in groups of eight words or less called records. Note that a record is actually one ECS word and therefore one record is obtained per memory cycle. Single 60-bit word transfers can also be effected. While one record is being transferred, the controller scans the other access channels for memory requests. If another channel is requesting access to ECS, that channel is serviced. If other channels are transferring data, each channel is serviced on a record basis. Thus, there may be time gaps between records on a given access channel.

The controller has the responsibility for timing the ECS banks. These banks are started into their memory cycle by the controller which must space the cycles so that data from one bank does not conflict with another. The controller also prevents two computers from requesting the same bank simultaneously by holding the latter request until the first has been satisfied. That is, the ECS Controller performs much the same function for ECS that Central Memory control does for Central Memory. The controller has registers to store the information that is received with each request so that no request is lost. The controller can process four requests concurrently.

Flag Register

The bits in this 18-bit register can be set or cleared by any computer attached to the controller. Its contents can also be compared with a new 18-bit word. However, the Flag register cannot be read directly. It can be accessed with little time penalty to a transfer that is in progress, or very rapidly when no other computer is using ECS.

Use of the Flag register is defined solely by the software and has no effect on the operation of the controller. For example, the Flag register can be used in a single or multi-computer system to indicate alert or priority conditions.

Parity Generator/Checker

For each 60-bit word to be stored in ECS, a parity bit is generated and stored along with that word (odd parity). Parity is checked on each 60-bit word as the storage word is disassembled after a Read operation. If a parity error occurs, a signal is sent to the coupler.

Extended Core Storage Couplers

The coupler is the CPU-controller interface. The 6600 coupler has hardware to add the relocation quantities to the basic address for both CM and ECS. If also performs the checks on Field Length. In the 6400 and 6500 systems these operations are done in the Central Processor.

6600 Coupler

In response to a Read or Write ECS instruction, the coupler performs the following operations:

1. Forms the initial ECS address and relays this address and the request and a Read or Write signal to the controller.

2. Checks the ECS address to see if it is in bounds.

3. Forms and checks the Central Memory address. This address is then sent to Central Memory.

4. Receives the word count and compares the number of words transferred with the word count to ensure transferring of the proper number of words.

5. As each eight-word record is transferred it increments the ECS address.

6. Generates an End of Transfer signal when the transfer is completed.

7. Sends a Go signal to Central Memory for every word to be read from Central Memory. (Central Memory control increments the Central Memory address during the transfer.)

8. Regulates data transfer rate for a 32K Central Memory which cannot sustain a transfer of one word every 100 nsec.

6400/6500 Coupler

In both systems only one coupler is used. In response to a Read or Write ECS instruction, the coupler performs the following operations:

1. Receives the initial ECS address and relays this address and a Request signal to the controller.

2. Receives the word count. The coupler compares the number of words transferred with the word count to ensure transferring the proper number of words.

3. As each eight-word record is transferred it increments ECS address once each eight-word record.

4. Generates an End of Transfer signal when the transfer is completed.

5. Sends a Go signal to Central Memory for every word to be read from Central Memory. (Central Memory control forms, checks, and increments the Central Memory address during the transfer.)

6. Regulates data transfer rate for a 32K Central Memory which cannot give a sustained transfer of one word every 100 nsec.

6416 Coupler

The 6416 coupler is similar to the 6400/6500 coupler but has some additional constraints imposed upon it. See 6416 Instructions, Part 2.

2. EXTENDED CORE STORAGE INSTRUCTIONS

These instructions provide the ability to communicate with ECS. The 6416 instructions are treated separately (see 6416 Instructions). The mnemonics used are those of the COMPASS assembly language.

6400/6500/6600 INSTRUCTIONS

011   *RE*   *Bj + K*   *Read Extended Core Storage*   *(30 Bits)*

fmi	j	K
59	51 50 48 47	30
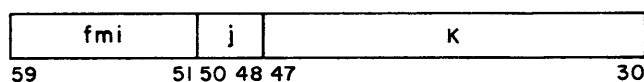
This instruction initiates a Read operation to transfer [(Bj) + K] 60-bit words from ECS to Central Memory. The initial ECS address is [(X0) + RA_{ECS}] ; the initial Central Memory address is [(A0) + RA_{CM}] .

012   *WE*   *Bj + K*   *Write Extended Core Storage*   *(30 Bits)*

fmi	j	K
59	51 50 48 47	30
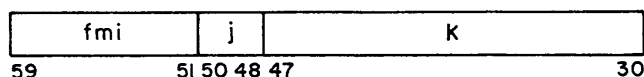
This instruction initiates a Write operation to transfer [(Bj) + K] 60-bit words from Central Memory to ECS. The initial Central Memory address is [(A0) + RA_{CM}] ; the initial ECS address is [(X0) + RA_{ECS}] .

Both instructions must be located in the upper-order position of the instruction word. Typical location of the ECS instructions in a program are in Figure 2-1. If an ECS instruction is not located in the upper-order position, the computer will exit to RA_{CM} regardless of the Exit mode bits. This also occurs if an ECS instruction is attempted in a system that does not have ECS.
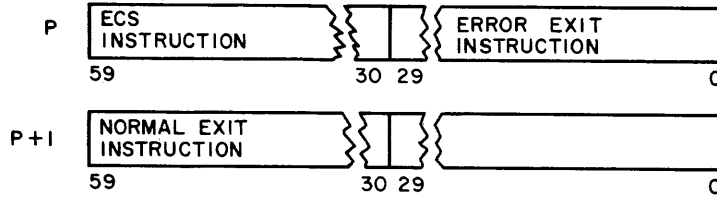
Figure 2-1. Instruction Locations

Either instruction in a system without ECS is illegal. For both instructions provision is made to inform the Peripheral and Control Processors that an ECS transfer is in progress. A 27, Read (P) Peripheral instruction can monitor the Central Processor Program Address register (P) by transferring its contents to the Peripheral and Control Processor A register. Either ECS instruction forces bit 17 of the P register to appear set to a 27 instruction. However, the bit is not set in the P register.

Address Formation

The starting address in ECS is formed by taking the truncated lower-order 24 bits of operand register X0 and adding this quantity to RA_{ECS}. In the addition, both quantities are taken as positive with the upper-order 36 sign bits (zeros) extended. In the 6400 and 6500 the upper 3 bits of RA_{ECS} do not exist; that is, it is a 21-bit quantity.

RA_{ECS} is the Reference Address within ECS, and FL_{ECS} is the alotted Field Length within ECS. Both are 24-bit quantities contained in the Exchange Jump package. When the program specified by this package is being executed, these quantities are held in registers in the Central Processor. The lower-order 6 bits (2^0 - 2^5) of the RA_{ECS} and FL_{ECS} registers do not exist. Therefore, the lower-order 6 bits in either of these 24-bit quantities always appear as zeros.

The starting address in Central Memory is formed by a similar process; the contents of address register A0 are added to RA_{CM}. RA_{CM} is the Reference Address within Central Memory, and FL_{CM} is the allotted Field Length within Central Memory. Both are 18-bit quantities contained in the Exchange Jump package.

Note that adding the Reference Addresses to (A0) and (X0) is accomplished automatically when the Read or Write instructions are executed. The relative addresses in A0 and X0, however, must be placed there by the program prior to executing the ECS instructions.

An example of a typical Read ECS operation follows:

EXAMPLE: Assume that a program starting at an inbounds address contains a Read ECS (011) instruction. The instruction specifies the number of words to be transferred as $(Bj) + K$. Prior to execution of this instruction, it it assumed that the program loaded registers Bj, A0, and X0 with the control parameters. Because the program was initiated by executing an Exchange Jump, the Central Processor holds the Reference Addresses RA_{CM} and RA_{ECS} and the Field Lengths FL_{CM} and FL_{ECS} as part of the Exchange Jump package.

It is desired, in this example, to transfer a block of 300_8 60-bit words from ECS to Central Memory. The various control parameters (octal) are assumed to be as follows:

(Bj)	= 100	RA_{ECS}	= 26500
K	= 200	FL_{ECS}	= 1600
RA_{CM}	= 1400	(A0)	= 4600
FL_{CM}	= 5300	(X0)	= 603

A map of Central Memory and ECS would then appear as indicated in Figure 2-2.
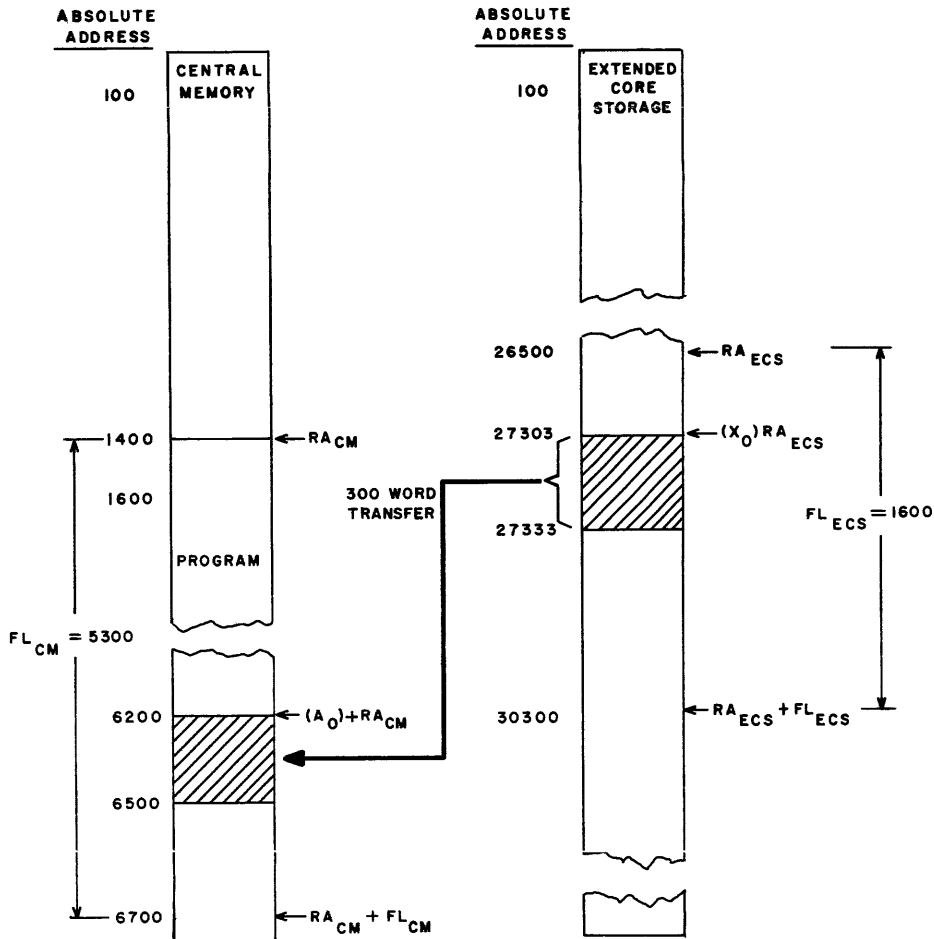
Figure 2-2. Memory Map (Read ECS Example)

A similar operation occurs for the Write ECS (012) instruction

For both Read and Write operations, the parameters held with the Central Processor which control the block transfer (namely Bj, X0, A0, RA_{CM}, RA_{ECS}, FL_{CM}, and FL_{ECS}), do not vary during the transfer. Therefore, an Exchange Jump occuring during a transfer may be effected. However, when the transfer program is again resumed, the transfer is started with the original parameters, and not from the addresses used just before the interruption in the program.

Address Range Faults

Three address range fault conditions can arise when executing the ECS communication instructions:

- Word count fault

- Central Memory address out of range

- ECS address out of range

1. Word Count

    If, in forming the word count $[(Bj)+K]$, the result is negative, an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at (P)+1 with no data transfer.

2. Central Memory Address

    Central Memory address out of range is checked by comparing FL_{CM} with the sum $[(A0) + (Bj) + K]$. FL_{CM} must be greater than this sum or an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at (P)+1 with no data transfer.

3. ECS Address

    ECS address out of range is checked by subtracting FL_{ECS} from the sum $[(X0) + (Bj) +K]$. In the comparison, FL_{ECS} is a 24-bit quantity with 36 upper-order bits of sign extended; X0 holds the 24-bit address quantity with 36 zeros occupying the upper-order bit positions. The result of this subtraction should always be negative; if positive, an address range fault occurs. If the Address Out of Range bit is set in the Exit Mode register, an error stop occurs; if this bit is clear, the Central Processor passes to the next instruction word at (P)+1 with no data transfer.

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Note that address range checks are made on the entire block of both ECS and Central Memory addresses before the transfer (Read or Write) is begun. If any address in the block to be transferred is out of range, either in Central Memory or ECS, no data is transferred, regardless of whether or not the Address Out of Range bit is set in the Exit Mode register.

Error Action

An error exit is an exit to the lower-order 30 bits of the instruction word containing the ECS Read or Write instruction. (These 30 bits would normally hold a jump to an error routine.)

Three error conditions cause an error exit:

1. Parity error(s) when reading ECS. If a parity error is detected, the entire block of data is transferred before the exit is taken. More than one parity error will result in only a single parity error exit.

2. The ECS bank to/from which data is to be transferred is not available because the bank is in Maintenance mode, or the bank has lost power.

3. An attempt to reference an address that is not available in the configured system.

In conditions 2 and 3 above the following occurs:

- On an attempted Write operation, no data transfer takes place and an immediate error exit is taken.

- On an attempted Read operation (and all addresses are in range) the Read operation proceeds but zeros are transferred to Central Memory.

Exchange Jump During ECS Transfers

If an Exchange Jump occurs while an ECS transfer is in progress, the exchange waits until completion of a record. Action is then as follows:

1. If the record just completed is the last record of the block transfer and the transfer was error free, the Central Processor exits to (P) + 1. The Exchange Jump then takes place.

2. If the record just completed is the last record of the block transfer and an error condition exists, the Central Processor exits to the lower instruction, executes it, and then the Exchange Jump is performed.

3. If the record just completed does not complete the block transfer, the transfer is terminated and the Exchange Jump is performed. A return Exchange Jump to this program begins execution with the ECS Read or Write instruction and restarts the transfer. Note the transfer does not resume at the point it was interrupted; rather, the entire transfer must be repeated.

Peripheral and Control Processors Read or Write During ECS Transfers

The Peripheral and Control Processors can access Central Memory during an ECS transfer. The Central Memory address requested by the Peripheral Processor is held by the coupler until the end of a record is reached. The coupler then stops all ECS action and allows the memory reference by the Peripheral Processor. When it is complete, coupler action proceeds as before. There is no effect on the ECS transfer other than the delay.

6416 INSTRUCTIONS

27   *RCS*   *d*   ***Read Extended Core Coupler Status***   *(12 Bits)*

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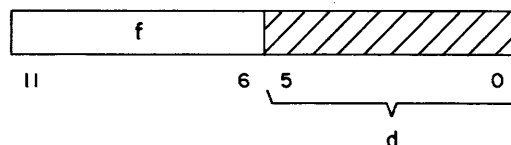
This instruction reads the 6416 ECS Coupler status and places these status bits in the upper-order 3 bits of the Peripheral and Control Processor A register. The significance of these status bits (when set to "1") is as follows:

Bit 17   ECS transfer is in progress.

Bit 16   Parity error(s) occurred during the last Read ECS operation.

Bit 15   At least one address of the last ECS transfer was not available (power off, in Maintenance mode, address not in system).

Within the ECS Coupler, status bit 17 is dynamic; bits 16 and 15 are cleared each time an ECS transfer is initiated.

26   **ECT**   *d*   ***Extended Core Transfer***   *(12 Bits)*

f	0	j
11	6 5	0

$$d$$
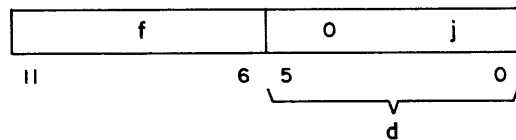
Execution of the ECS Transfer instruction initiates memory operations by transmitting an 18-bit address, 'n', from the Peripheral Processor A register to the 6416 16K memory. Address "n" holds a parameter word (Figure 2-3).

X_0	A_0	K
59 36	35 18	17 0
STARTING ADDRESS IN EXTENDED CORE STORAGE	STARTING ADDRESS IN 16K MEMORY	WORD COUNT
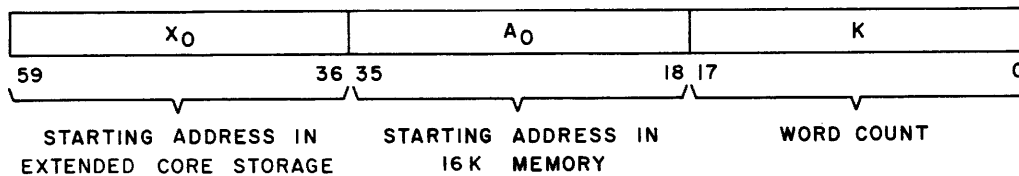
Figure 2-3. ECS Parameter Word

The 'd' portion of this instruction specifies the storage operation to be performed:

If 'j' = 0, Read 'K' words from ECS into 16K memory.

If 'j' = 1, Write 'K' words from 16K memory into ECS.

NOTE

If this instruction is executed without ECS in the
system configuration, it acts as a Pass (do-nothing)
instruction.

Note that addresses contained in the word at address 'n' are absolute addresses.
Operating systems may require relocation (adding RA to an address) and Field
Length testing, e.g., is "address + (Bj + K)" $\leq$ FL? (The Exchange Jump package
contains RA and FL values for Central Memory and for ECS.) The 6416 has no
hardware for automatic relocation and Field Length testing; it is therefore incumbent
upon the program to perform these functions whenever required by an operating
system.

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3. EXTENDED CORE STORAGE ADDRESSING

ADDRESS FORMATS

The address format varies with the ECS configuration used (Figure 3-1). Addresses
are phased so that consecutive addresses go to consecutive banks. The lowest 3 bits
of any address are used to disassemble the 488-bit ECS word into 60-bit data words
(and their associated parity bits). On a system of 250K or more (two or more banks),
the next bits will select the bank. Up to 4 bits are provided to select 16 banks (or
four bays). The next 14 bits select one 488-bit word in the selected bank. The
remaining bits are not used for addressing purposes but serve other functions. First,
they are used to check for illegal addresses; second they are used to perform Flag
register operations.

If the illegal address bits (Table 3-1) are set, they will cause an error exit as
specified under Error Action.

TABLE 3-1. ILLEGAL ADDRESS BITS

CONFIGURATION	BIT NUMBER
125K	17
200K	18
500K	19
1000K	20
2000K	21
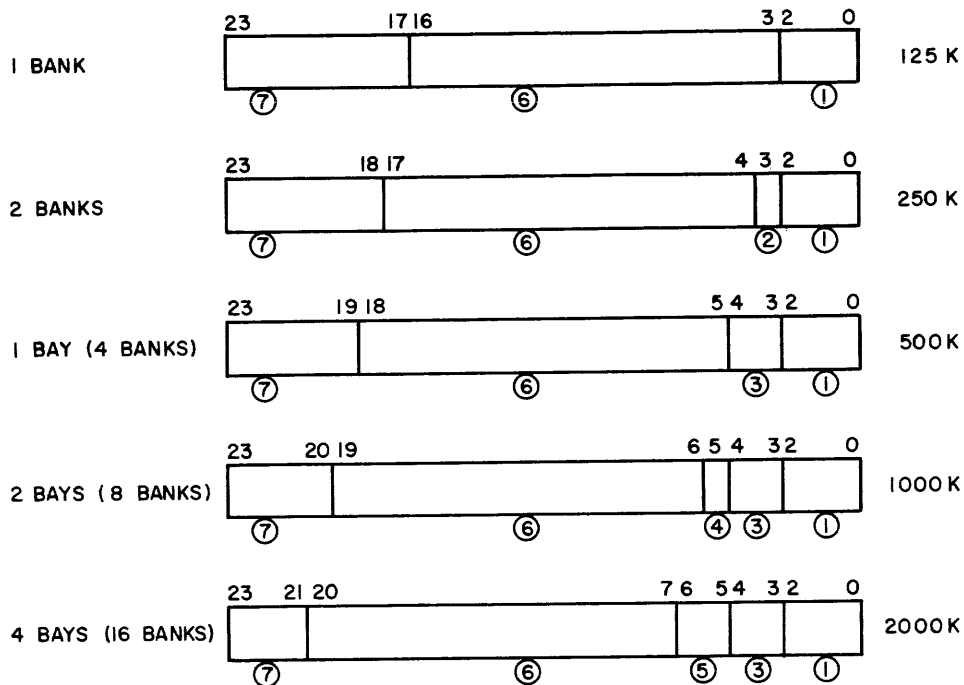
Figure 3-1. ECS Formats

FLAG REGISTER OPERATION

The controller has an 18-bit Flag register to allow programs to provide information about the current or previous operations with any computer. One of its uses could be analogous to a reserved status word being maintained in ECS but available at far greater speed, since ECS references are not made. The register cannot be read directly; instead, a computer may interrogate it and/or write into it.

Flag Register Selection

The Flag register is selected by executing an ECS Read or Write instruction with bit 23 set in both the ECS address (X0) and FL_{ECS}. No Field Length checking is performed and RA_{ECS} is not added to the ECS address (X0). The operation is the same for either ECS instruction and is not affected by the Fifty Percent Capacity Reduction.

The contents of X0 are sent to the controller as is any other ECS address. Since bit 23 is set, the controller recognizes this as a Flag register operation. It then translates bits 22 and 21 to see what function is to be performed.

The response to a Flag register function is either an error exit or a normal exit from the ECS instruction.

For a Flag register operation the ECS address is considered to have three parts (Figure 3-2).

```
FUNCTION                    FLAG
CODE                        WORD

  ┌───┬─────┬──────────────────────────────────┐
  │ N │/////│                                  │
  └───┴─────┴──────────────────────────────────┘
  23   21 20  18 17                            0
```
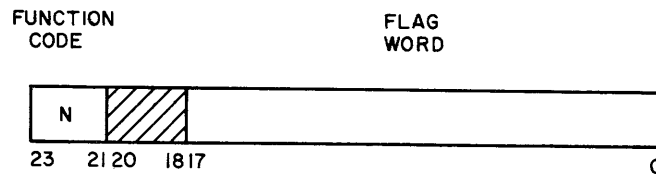
Figure 3-2. ECS Address (X0) Format for Flag Register Operation

1. Function Code (N) is bits 21-23. Bit 23 is always set for a Flag register operation.

2. Bits 18-20 are not used.

3. The flag word is bits 0-17. These bits are compared with or entered into the Flag register depending on the function specified by N.

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Flag Function Codes

Four operations can be specified by bits 21 and 22.

1. N=4; Ready/Select. A bit by bit comparison is made between the contents of the Flag register and the flag word. If all the set bits in the flag word are cleared in the Flag register, a positive comparison has been made and all the set bits in flag word are entered into the Flag register. Note that the cleared bits in the flag word have no effect on the Flag register. On a comparison, coupler action terminates as though a data transfer has been completed; that is, a normal exit.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 010
flag word   = 101

This is a positive comparison so the Flag register is changed.
Final contents of Flag register = 111

If a positive comparison is not made, the Flag register remains unchanged but an error exit is taken by the computer.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 010
flag word   = 111

This is a negative comparison so the Flag register is unchanged.
Final contents of Flag register = 010

2. N=5; Selective Set. No comparison is made. All set bits in the flag word are set in the Flag register. The coupler then terminates the transfer and unconditionally exits to the next instruction.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 010
flag word   = 100
Final contents of Flag register = 110

3. N=6; Status. This is the same as a Ready/Select code but the Flag register is not changed on a positive comparison. The comparison is made in the same manner and the exit conditions are the same.

4. N=7; Selective Clear. No comparison is made. All set bits in the flag word are cleared in the Flag register. The coupler then terminates the transfer and unconditionally exits to the next instruction.

EXAMPLE: (only 3 bits are shown)

Initial contents of Flag register = 110
flag word   = 101
Final contents of Flag register = 010

FIFTY PERCENT CAPACITY REDUCTION

The system can be reduced to half of the configured capacity by a switch in the controller.* This is done by left shifting some address bits by one position (Table 3-2). This means that one of the Bank selection bits in the controller address register is not used. This bit is set or cleared, depending on which half of the system is to be used. With the bit set, the upper half of the addresses are available; with the bit cleared, the lower half of the addresses are available. The selection is made by a second switch on the controller.

_____

*With the exception of the 125K system.

The capacity reduction is done per channel. It is therefore possible to degrade two channels and assign complementary halves of ECS to each channel. For example, in a 500K system, 250K could be assigned to channel 1 and the other 250K assigned to channel 2. The Flag register operations are not affected by the capacity reduction.

TABLE 3-2. ADDRESS SHIFTING

CONFIGURATION	BITS SHIFTED		SELECTION BIT
	FROM:	TO:	
250K	3-17	4-18	3
500K	4-18	5-19	4
1000K	5-19	6-20	5
2000K	6-20	7-21	6

Figure 3-3 shows a typical address shifted by the fifty percent capacity reduction.
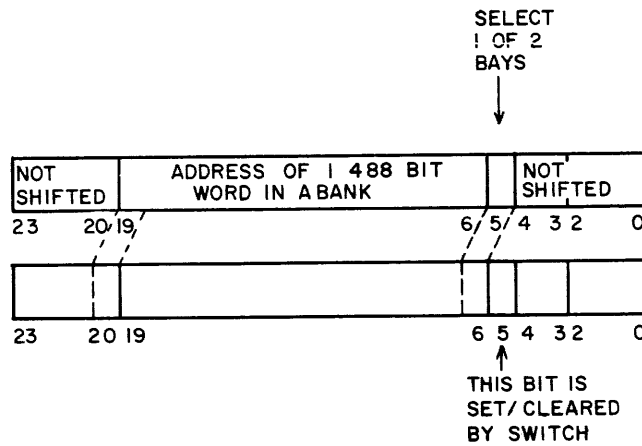
Figure 3-3. Example of Address Shifting for 1000K

4. TRANSFER RATES

Two major factors affect the transfer rate of an ECS system; 1) the memory size of ECS and CM in the system, and 2) the system conflicts which occur on the ECS level and the Central Memory level.

MEMORY SIZE

Extended Core Storage Size

To achieve the maximum transfer rate, four banks (500K) of ECS must be performing back to back memory references with each bank staggered 800 nsec apart. This gives four ECS records every 3.2 μsec; that is, 32 60-bit words every 3.2 μsec or one word per 100 nsec. The coupler must request memory every 800 nsec and furthermore must be phasing its addresses. ECS configurations that are larger than 500K do not increase this maximum transfer rate.

If ECS has two banks (250K), the controller will allow the first two requests but a third request will encounter a busy ECS bank. This request must wait until a bank becomes free. This gives an effective transfer rate of two ECS records per 3.2 μsec or one word every 200 nsec. The data words are transferred in a pattern of one word every 100 nsec for 1600 nsec, wait 1600 nsec, transfer another 16 words, and so on.

If ECS has one bank (125K), the controller will allow the second request only after the first memory cycle is complete. This gives an effective transfer rate of one ECS record per 3.2 μsec, or one word every 400 nsec. The data words are transferred in

Rev A

a pattern of eight words every 100 nsec for 800 nsec, wait 2400 nsec, transfer another eight words, and so on.

Central Memory Size

At least 65K of Central Memory is required to sustain a one word per 100 nsec transfer rate. If less Central Memory is available, the coupler must request ECS at a slower rate.

If a 32K Central Memory is used, the coupler requests ECS at 1-μsec intervals. The data words are transferred in a pattern of one word every 100 nsecs for 800 nsec, wait 200 nsec, transfer another eight words, and so on. This gives an effective transfer rate of one word every 125 nsec. This presumes that the ECS is of sufficient size to be capable of transferring data at this rate.

If a 16K Central Memory is used, the coupler requests ECS at 1-μsec intervals again. However, it accepts only the first four words of the ECS record. The coupler then sends another request for the second four words. Since only half of an ECS record is transferred, the 16K memory will send two consecutive references to the same ECS bank. Therefore, for each pair of half records, the data is transferred as follows: transfer one word every 100 nsec for 400 nsec, wait 3.2 μsec (one memory cycle), and transfer another four words. If ECS has only one bank, the 16K memory must wait another 3.2 μsec; that is, transfer four words, wait 3.2 μsec and so on. This gives an effective transfer rate of one word every 800 nsec.

If ECS has two or more banks, there is no need for the 16K memory to wait 3.2 μsec for the second eight-word ECS record. The data is then transferred in the following pattern: transfer four words, wait 3.2 μsec, transfer four words, wait 800 nsec, transfer four words, wait 3.2 μsec, transfer four words, wait 800 nsec, and so on. This gives an effective transfer rate of one word every 500 nsec.

Table 4-1 lists the transfer rates for one computer using an ECS system and with no other computers requesting ECS.

TABLE 4-1. TRANSFER TIMES FOR ONE 60-BIT WORD (NSEC)

CENTRAL MEMORY SIZE	ECS SIZE				
	125K	250K	500K	1000K	2000K
16K	800	500	500	500	500
32K	400	225	125	125	125
65K	400	200	100	100	100
131K	400	200	100	100	100

SYSTEM CONFLICTS

Two types of conflicts may occur in the controller when there is more than one computer in the system. The first type of conflict occurs when data transfers are attempted; the second type occurs during Flag register operations. These conflicts only occur during simultaneous requests. If only one computer is requesting ECS, no conflicts occur.

Extended Core Storage Data Conflicts

With N computers the maximum simultaneous transfer rate for any one of the computers is 1/N of the maximum ECS transfer rate (where N may be 1, 2, 3, or 4).* For 125K ECS, this is always the transfer rate. For systems larger than 125K, this assumes that the requests are not for the same bank. The following times assume a Central Memory size that can transfer data at the maximum speed. Computers with smaller Central Memories will not realize as much performance degradation. Any time the requests are for the same bank, system performance drops to that of a

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*This assumes all computers are of the same CM size.

125K ECS while these requests are present. That is, the worst case transfer rate that ECS itself can deliver is 1/N of its maximum rate.

A less common delay can occur when one computer requests a Write operation and that request is then followed immediately by a read request from a second computer. Instead of waiting the normal 800 nsec between requests the second computer waits 1600 nsec. Accurate estimates of transfer times can be gained by using the flow chart in Appendix A.

Flag Register Conflicts

Because of the inefficiency of allowing more than one computer to request ECS at the same time, the controller has a Flag register available which can be used by the software to coordinate the ECS transfers. The following discussion demonstrates the advantages of using the Flag register as a status register.

Assume a transfer is underway; a second computer can perform a Flag register operation on a pre-defined bit which may inform it that ECS is being used. This will delay the actual data transfer by only 300 nsec minimum and by 3.5 μsec (worst case). If a second and third computer are also requesting Flag register operations, the controller will perform them before returning to the data transfer. In this case, the second and third computers will add only 300 nsec each to the original delay of 3.5 μsec.

Assume four 65K computers using a 500K ECS System. Assume that each computer wishes to transfer 5000 data words from ECS; that is, a total of 20,000 words.

If all four are allowed to request ECS at the same time, the effective transfer rate as it appears to any one computer is one 60-bit word every 400 nsec, even though ECS is running at full speed. Since there is a total of 20,000 words to be transferred, the total transfer time for all four computers is 2 ms. This is the best case and ignores the conflicts due to requesting the same bank. In this example, bank conflicts

could occur a significant percentage of the time; therefore, the calculated transfer time of 2 ms is less than the actual time required. Worst case transfer time is 400 nsec multiplied by 20,000 words or 8 ms.

Assume now that the transfers are sequential with one machine transferring data and the other three performing Flag register operations to status ECS. Assume also that these Flag operations are done every 50 μsec; also, the Flag operations are not performed back to back but instead each one incurs an average penalty of 1.6 μsec. The operation then takes 300 nsec. This means there is a total of 1.9 μsec penalty for each Flag operation.

Without an interruption the first machine would take 500 μsec to transfer the data. However, each of the other machines would interrupt the transfer 10 times; a total of 30 in all. This would add 57 μsec (30 x 1.9 μsec) to the first 5000 word transfer, giving 557 μsec. Note that there will be only two machines doing Flag operations during the second 5000 words, one machine during the third 5000 words and none during the last 5000 words. Therefore, the total transfer time will be:

$$(500 + 57) + (500 + 38) + (500 + 19) + (500) \ \mu sec*$$

This gives a total of 2.114 ms. This is only slightly more than the best case time and a considerable improvement over the worst case time of 8 milliseconds. It should be noted that the systems performance is further enhanced because the first computer can start using its data only 557 μsec after starting a transfer. This is in marked contrast to the 2-ms delay when the Flag register is not used.

The Flag register can be used to advantage on improving the total transfer rate of the ECS system but it is particularly useful where priority transfers are necessary.

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*This ignores the initial access time.

Central Memory Conflicts

Central Memory conflicts occur when a Peripheral and Control Processor attempts to use Central Memory during an ECS transfer.

Provision is made to allow a Peripheral and Control Processor access to Central Memory during an ECS transfer. There is a delay of 1 μsec plus the ECS access time every time this occurs.* However, it can occur only between eight-word records and only one memory reference is allowed. Therefore, in a worst case condition, a delay of 1 μsec for every eight words transferred could occur. This delay can be readily minimized by checking the status bit which appears set in the Central Processor P register during an ECS transfer (see 6400/6500/6600 Instructions, page 2-1).

ACCESS TIMES

6600 Computer

For the 6600, the access time is dependent upon Central Memory being free and all functional units being released. Once these conditions are met, 1.6 μsec is required by the Central Processor and the coupler before a request is sent to the controller. A further 1.8 μsec are required before the first data word is received (on a Read operation). This portion of the access time can be increased by the conflicts that affect transfer times.

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*See Access Time.

6400/6416/6500 Computers

These computers do not have to wait for functional units to be released but do have to wait for CM to be quiet. Once this condition is met, 3 μsec is required by the Central Processor and the Coupler before a request is sent to the controller. A further 1.8 μsec are required before the first data word is received (on a Read operation). This portion of the access time can be increased by the conflicts that affect transfer times.
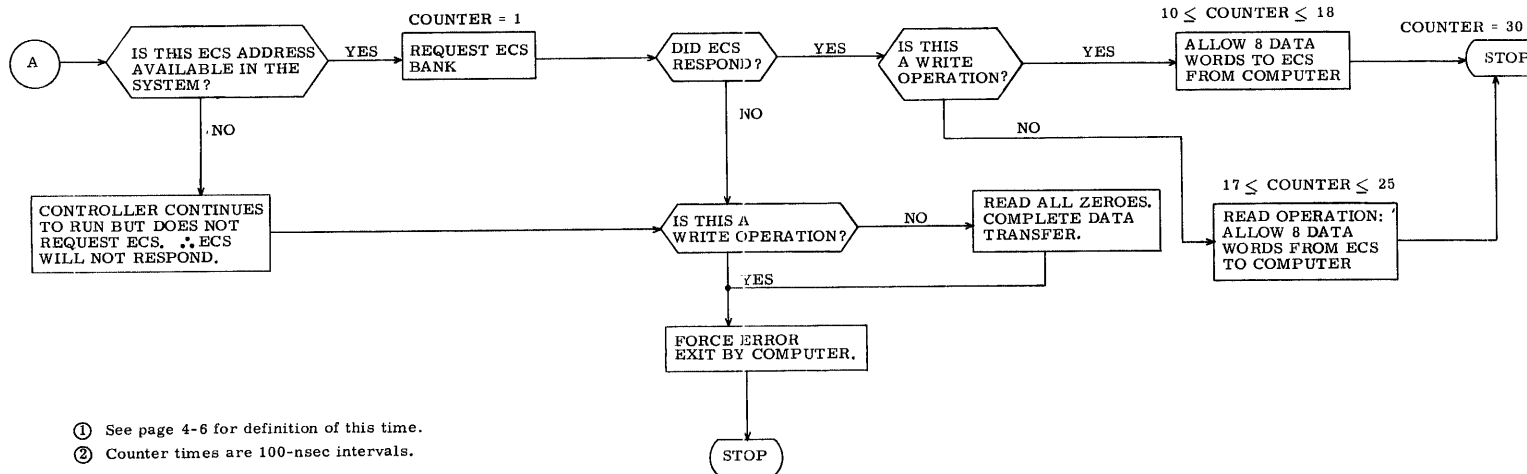
Appendix A

TRANSFER TIMING

TRANSFER TIMING

The flow chart shows the controller's sequence for one request from the computer. The controller can have four concurrent requests. This is necessary because four banks of ECS must be in operation to maintain the maximum transfer rate.

For each request, the controller retains the address of the selected bank and the channel that originated the request. The controller contains four counters that sequence controller activity. One counter is assigned to each request. Each counter is started when a request is sent to ECS and runs 200 nsec ahead of the read/write cycle counter in the bank. For normal transfers, each counter would start 800 nsec after the previous one; that is, when that counter equals 8. All conflicts in the controller delay the starting of the counter for the current request. The coupler waits until the controller starts its counter. When a Flag register operation occurs, the counter is never started.

RECEIVE ADDRESS, REQUEST AND READ/ WRITE SIGNAL.

①

IS THIS A FLAG REGISTER OPERATION?

NO

ARE THERE ANY OTHER REQUESTS?

NO

COUNTER = 0

INFORM COUPLER THAT REQUEST IS ACCEPTED. START COUNTER ASSIGNED TO THIS REQUEST.

②

A

YES

WAIT FOR PREVIOUS REQUESTS TO BE COMPLETED. MAXIMUM WAIT IS 3.2 μSEC PER REQUEST.

YES

IS THIS REQUEST FOR THE SAME BANK AS ANY OF THE PREVIOUS REQUESTS?

YES

WAIT UNTIL BANK IS FREE. MAXIMUM WAIT IS 3.2 μSEC PER REQUEST FOR THAT BANK.

WAS WAIT LESS THAN 1.6 μSEC?

NO

YES

PERFORM FLAG OPERATION

NO

IS THIS OPERATION A WRITE?

NO

WAIT UNTIL PREVIOUS COUNTER ≥ 8. MAXIMUM WAIT IS 0.8 μSEC.

FORCE NORMAL EXIT OR ERROR EXIT DEPENDING ON FLAG RESULT.

YES

NO

WAS REQUEST BEFORE THIS A READ?

YES

STOP

WAIT UNTIL PREVIOUS COUNTER ≥ 16. MAXIMUM WAIT IS 1.6 μSEC.

A

IS THIS ECS ADDRESS AVAILABLE IN THE SYSTEM?

YES

COUNTER = 1

REQUEST ECS BANK

DID ECS RESPOND?

YES

IS THIS A WRITE OPERATION?

YES

10 ≤ COUNTER ≤ 18

ALLOW 8 DATA WORDS TO ECS FROM COMPUTER

COUNTER = 30

STOP

NO

NO

NO

CONTROLLER CONTINUES TO RUN BUT DOES NOT REQUEST ECS. ∴ ECS WILL NOT RESPOND.

IS THIS A WRITE OPERATION?

NO

READ ALL ZEROES. COMPLETE DATA TRANSFER.

17 ≤ COUNTER ≤ 25

READ OPERATION: ALLOW 8 DATA WORDS FROM ECS TO COMPUTER

YES

FORCE ERROR EXIT BY COMPUTER.

STOP

① See page 4-6 for definition of this time.
② Counter times are 100-nsec intervals.

Appendix B

ECS OPTIONS

ECS OPTIONS

The descriptions of the options are intended only as a guide. Complete information is available from Control Data representatives.

STANDARD OPTIONS

The following options add the ECS coupler logic to the computer.

10101   Conversion kit for 6400. Converts a 6404 to a 6614 or a 6405 to a 6415. Includes coupler logic enabling the central computer to communicate with the ECS controller.

10102   Conversion kit for 6600. Converts a 6601 to a 6613 or a 6604 to a 6614. Includes coupler logic enabling the central computer to communicate with the ECS Controller.

The following options are to increase the memory size of the central computer. They also add the ECS Coupler logic to the computer.

10106   Converts a 6604 to a 6613.

10113   Converts a 6405 to a 6414.

10120   Converts a 6404 to a 6413.

The following option adds a second Central Processor to a 6400. It also adds the ECS Coupler logic to the computer.

10113   Converts a 6404 to a 6514.

The following options add the Central Exchange Jump and Monitor Exchange Jump instructions to the computer.

10103   Adds the CEJ/MEJ instructions to all 6400 or 6500 computers with the exception of the 6416.

10104   Adds the CEJ/MEJ instructions to the 6613, 6614, and 6615 computers.

SPECIAL OPTIONS

The following options add only the ECS Coupler logic to the computer.

60080   Adds ECS Coupler to 6613, 6614, and 6615 computers.

60081   Adds ECS Coupler to 6413, 6414, 6415, and 6416 computers.

COMMENT SHEET

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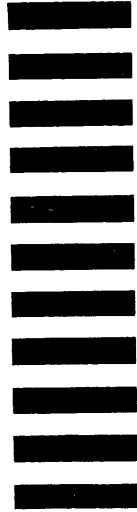
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